REMARKS

This responds to the Office Action mailed on April 19, 2007.

No claims are amended or canceled, and no claims are added in the present Response to the Office Action. As a result, claims 7-10, 12-15, 19-25, and 27-32 remain now pending in this application.

§102 Rejection of the Claims

Claims 7-10, 12-15, 19-25, and 27-32 were rejected under 35 USC § 102(e) as being anticipated by Thompson (U.S. 2003/0237070 A1, hereinafter referred to as "Thompson"). Applicant traverses the rejection of these claims for the reasons stated below and more.

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added).

Independent claim 7 is not anticipated.

Independent claim 7 recites (with emphasis added):

> 7. A method of software pipelining for improving efficiency of loops handling, the method comprising:
>
> checking for availability of rotating registers to hold computed values that are live across multiple stages in a software-pipelined loop;
>
> and spilling and filling the computed values held in rotating registers in a software-pipelined loop **using rotating stack memory locations for rotating registers**, when there are no rotating registers available to hold the computed values, wherein **the number of the rotating stack memory locations used for spilling and filling the computed values is equal to the number of simultaneous live values generated by the rotating register**.

The Office Action incorrectly argues that paragraph [0014] of Thompson discloses "spilling and filling the computed values held in rotating registers in a software-pipelined loop using rotating stack memory locations for rotating registers" as recited in claim 7.

Referring to paragraph [0014] of Thomson, which was relied upon by the Office Action (with emphasis added):

> ... If a situation occurs in which a register is not available to perform an operation when required by the optimized schedule, it is necessary to "spill" one or more registers. That is, **the contents of the spilled registers are temporarily moved to RAM to make room for the operations that must be performed, and moved back again when the register bottleneck is alleviated**. As previously noted, the process of moving register contents (i.e., information) to and from RAM is relatively time consuming and thus tends to undermine the efficiencies that may be realized using instruction schedule optimization ... *(emphasis added)*

Clearly, it can be seen that paragraph [0014] of Thomson merely mentions "the contents of the spilled registers are temporarily moved to RAM" and "moved back again when the register bottleneck is alleviated." But paragraph [0014] of Thompson fails to disclose "spilling and filling the computed values held in rotating registers in a software-pipelined loop **using rotating stack memory locations for rotating registers"** as recited in claim 7. Applicant contends that Thompson does not disclose the rotating stack memory feature as recited in claim 7 either. Thus, Thompson fails to disclose the feature "spilling and filling the computed values held in rotating registers in a software-pipelined loop using rotating stack memory locations for rotating registers" as recited in claim 7.

Additionally, the Office Action incorrectly states the statement that "... live ranges are less or equal to the initial interval ..." of paragraph [0055] of Thompson discloses a feature "the number of the rotating stack memory locations used for spilling and filling the computed values is equal to the number of simultaneous live values generated by the rotating register" as recited in claim 7. Because Thompson, as discussed above, does not mention the feature "using **rotating stack memory locations** for rotating registers" as recited in claim 7, Thompson cannot possibly disclose the feature "**the number of the rotating stack memory locations** used for spilling and filling the computed values is equal to the number of simultaneous live values generated by the rotating register".

Further, it appears to Applicant that the Office Action cites paragraph [0055] of Thompson, while intending to cite paragraph [0054]. Referring to paragraph [0054] of Thompson, (with emphasis added)

> ... The live range examiner determines the active variables over a present program loop of interest. In turn the active variables are further processed by logic that determines when identified **live ranges are less than or equal to the initiation interval** of the present program loop of interest. As indicated in the schematic, variables with live ranges that do not extend beyond the initiation interval 712 are forwarded to a surplus rotating register allocator, where the variables are applied to rotating registers and the result reported via rotating usage information 634. Conversely, variables with live ranges that exceed the initiation interval are forwarded to allocator 720. Allocator 720 applies these variables and reports the results via rotating register allocations 632. If during the process of allocating rotating registers, the allocator 720 is unable to meet the demands of the modulo schedule 622 for rotating registers, the insufficient rotating register corrector 730 is so informed. The insufficient rotating register corrector 730 adjusts the modulo schedule 620 accordingly. *(emphasis added)*

It can be seen that "**live ranges are less than or equal to the initiation interval**" of paragraph [0054] of Thompson fails to disclose the feature,

> "**the number of the rotating stack memory locations used for spilling and filling the computed values is equal to the number of simultaneous live values generated by the rotating register**" (emphasis added)

as recited in claim 7, because paragraph [0054] of Thompson merely shows "variables with live ranges that do not extend beyond the initiation interval 712 are forwarded to a surplus rotating register allocator," and "conversely, variables with live ranges that exceed the initiation interval are forwarded to allocator 720". Applicant believes that Thompson does not mention the number of rotating stack memory locations at all. Thus, Applicant respectfully submits that Thompson does not disclose the feature,

> "the number of the rotating stack memory locations used for spilling and filling the computed values is equal to the number of simultaneous live values generated by the rotating register"

as recited in claim 7.

Therefore, for at least these reasons, Thompson does not disclose each and every element of claim 7. Accordingly Thompson fails to anticipate claim 7.

Independent claim 10 is not anticipated.

Independent claim 10 recites (with emphasis added):

> 10. A method of software pipelining for improving efficiency of loop handling, the method comprising:
>
> checking for availability of FP rotating registers to hold FP computed values that are live across multiple stages in a software-pipelined loop; and
>
> **spilling and filling the computed values using rotating integer registers for holding addresses of stack memory locations when there are no FP rotating registers available to hold the computed value,** the spilling and filling the computed values comprising:
>
> checking for availability of N+1 rotating integer registers, wherein N is number of stages a computed value that needs to be spilled is live in the software-pipelined loop; and
>
> spilling and filling the computed value in stack memory locations whose addresses are held in corresponding N+1 rotating integer registers, when the N+1 rotating integer registers are available.

The Office Action incorrectly argues that FIG. 6B, 660 and related text disclose a feature "**spilling and filling the computed values using rotating integer registers for holding addresses of stack memory locations when there are no FP rotating registers available to hold the computed value**" as recited in claim 10. Applicant disagrees. Referring to [0053] of Thompson, which describes FIG. 6B,

> As indicated in the schematic diagram of FIG. 6B, the modulo schedule instruction generator 650 receives information from the register spiller 640, the rotating register allocations 632, the modulo schedule 622, and the low-level IR with NOPs 512. The modulo schedule instruction generator 650 constructs a rotating register IR 652 (i.e., another representation of the source code 150) from the inputs and forwards the rotating register IR 652 to a static register allocator and memory spiller 660. The static register allocator and memory spiller 660 uses the rotating register IR 652 and the rotating register usage information 634 to determine when it is appropriate to assign static or global variables to rotating registers. The static register allocator and memory spiller 660 generates a static register IR (i.e., a representation of the source code 150). In this way, the modulo scheduler and register allocator 540 takes advantage of available rotating register resources during the loop of interest. The modulo scheduler and register allocator 540 forwards the rotating register IR 652 and the static register IR 662 to the machine code generator 670, which in turns creates machine level code 152.

It can seen clearly that the above cited paragraph [0053] does not disclose the feature,

"spilling and filling the computed values using rotating integer registers for holding addresses of stack memory locations when there are no FP rotating registers available to hold the computed value"

as recited in claim 10. Paragraph [0053] of Thompson does not even mention a presence of any rotating integer register at all, thus cannot possibly disclose a feature **"using rotating integer registers for holding addresses of stack memory locations"** as recited in claim 10. Applicant further contends that Thompson also fails to disclose the feature **"spilling and filling the computed values using rotating integer registers for holding addresses of stack memory locations when there are no FP rotating registers available to hold the computed value"** as recited in claim 10. Thus, for at least these reasons, Thompson fails to disclose each and every element of claim 10, accordingly does not anticipate claim 10.

Independent claims 14, 18, 21, 27 and 30 are not anticipated.

The reasons discussed for independent claim 10 also apply to independent claims 14, 18, 21, 27, and 30. Thus, independent claims 14, 18, 21, 27, and 30 are not anticipated by Thompson.

Each of claims 8-9, 12-13, 15, 19-20, 22-25, 28-29, and 31-32, directly or indirectly, depends on one of independent claims 1, 10, 14, 18, 21, 27 and 30, thus each dependent claim includes all the features of the independent claim on which it depends. Therefore, for at least the reasons discussed above for the independent claims, Thompson fails to anticipate these dependent claims either.

Accordingly, Applicant respectfully requests reconsideration and allowance of claims 7-10, 12-15, 19-25, and 27-32.

RESERVATION OF RIGHTS

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6970) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date May 29, 2007

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 29th day of May 2007.

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